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EQUIVALENT CIRCUIT OF UNSYMMETRICAL
INDUCTANCE DIODE USING LINVILL LUMPED MODEL

BY
Lawrence
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A

THESIS

submitted to the faculty of the

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Degree of

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ABSTRACT

Integrated circuit techniques and applications are rapidly changing the electronics industry. A problem common to both state-of-the-art approaches to integrated circuit fabrication is that of miniaturizing and integrating inductors.

It is found that, for a certain range of injection current levels, certain unsymmetrically doped junction diodes have an inductive small-signal impedance. This thesis discusses the theory of inductance diodes and applies finite difference equations and the Linvill lumped model to the differential equations that describe their carrier flow processes. The static I-V characteristic and the small-signal equivalent circuit at high injection densities are derived. The elements (R,L,C) of this equivalent circuit are given in terms of the Linvill parameters. Impedance calculations are made using this equivalent circuit and are in satisfactory agreement with experimental results for diodes in which the base length is not too long compared to the diffusion length.

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Thanks go to the Metallurgical Engineering Department for providing the metallurgical stage microscope.

The author expresses his sincere appreciation to his wife for typing the original copy.

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LIST OF SYMBOLS

A	...	diode cross sectional area
\AA		
A	...	angstrom unit
C	...	capacitance
C_J	...	junction capacitance
d	...	diode base length
D	...	effective diffusion constant
D_n	...	diffusion constant for electrons
D_p	...	diffusion constant for holes
e	...	magnitude of electronic charge unit
\mathcal{E}	...	electric field intensity
h	...	henry (unit of inductance)
H_c	...	combinance
H_n	...	electron diffusance
H_p	...	hole diffusance
I	...	current
I	...	intrinsic region
I_n	...	electron current
I_p	...	hole current
j_n	...	electron current density
j_p	...	hole current density
J	...	junction
k	...	Boltzmann's constant
L	...	inductor
L_p	...	diffusion length for holes
M_n	...	electron mobility

M_p	...	hole mobility
n	...	region of semiconductor with excess electrons
n	...	mean density of electrons
n_i	...	excess density of electrons at point i
n_n	...	electron density in n-region
n^+	...	heavily doped n-region
N	...	n-type semiconductor
N	...	carrier concentration
N_d	...	ionized impurity density
p	...	region of semiconductor with excess holes
p	...	mean density of holes
p_i	...	excess density of holes at point i
p_n	...	hole density in n-region
p^+	...	heavily doped p-region
P	...	p-type semiconductor
Q	...	quality factor
R	...	resistance
R	...	infinite recombination velocity center
R_b	...	base resistance
S	...	stomach
T	...	absolute temperature
V	...	voltage
V_J	...	junction voltage
x	...	distance along length of semiconductor bulk
\bar{Z}	...	impedance
α	...	short circuit current transfer ratio
σ	...	conductivity

μ ... mobility of current carriers

μ_n ... electron mobility

μ_p ... hole mobility

τ_p ... lifetime of holes

ω ... angular frequency

bar over symbol indicates complex or phasor quantity

CHAPTER I

INTRODUCTION

A. Microelectronics.

The term microelectronics means any device-and-circuit technology that allows complete electronic functions to be performed by a very small module or device package. Microelectronics encompasses the wide spectrum of modern-day electronics advancements under the varied labels of microminiaturization, molecular electronics, microcircuits, thin films, chip and multi-chip circuits, integrated circuits and others. The technology and name that is presently forging ahead as the state-of-the-art is integrated circuits. Although integrated circuits include a family of fabrication techniques, there are only two basically different processes. These generic processes, utilizing entirely different design and fabrication principles, are the silicon monolithic process and the thin film process. The root of the term monolithic may be traced to the Greek: mono--meaning single, and lithos--meaning stone. A monolithic circuit is a circuit fabricated from a single stone, or single crystal. The silicon-diffused monolithic circuit consists of a number of circuit elements, both active and passive, diffused into a continuous body of single crystal silicon substrate. The term thin film as it applies to integrated circuits is quite ambiguous. The film refers to the coating of dielectric, resistive, conductive, or semiconductive material that is deposited on a passive substrate such as glass or ceramic. Used correctly, thin film defines layer thicknesses in the range from one monolayer (about 5 \AA) to approximately 1 micron. Any film of larger

thickness dimension should be referred to as thick film. In integrated electronics, it is common to term every deposited layer a thin film even though it be a mil or more thick. The thin film circuit consists of a number of circuit elements, again active as well as passive, deposited in a patterned relationship on the structural supporting substrate material.

The two leading techniques of integrated circuit fabrication are variations of these generic processes. One of these is a modification of the silicon-diffused monolithic approach. The other is a hybrid arrangement using deposited thin films for the passive components and discrete active devices formed by diffusion or related processes. The modified monolithic technique is still basically an all-diffusion process but uses some type of isolation technique in order to minimize component interaction. Recent success in isolating component parts of the monolithic structure by using an insulating material layer of SiO_2 suggests that dielectric isolation will be the method of the future (Aarons 1965, Allison 1965).

Although monolithic and hybrid circuit techniques have different characteristics, each has its unique and individual superiorities. The competition between the two is high and is creating a platform of discussion in the Solid-State Industry. A recent major conference, The 1965 International Solid-State Circuits Conference, featured a keynote panel discussion entitled "Hybrid Versus Silicon Monolithic Circuits" (Davis and Sack 1965). Whatever the merits of either technology, they have at least one

stumbling block common to both. This is the inductance parameter. Inductance coils of reasonable Q and suitable for tuned-circuit applications defy miniaturization to the integrated circuit level. Ingenuity in circuit design, either to eliminate the need of inductance or alternately to simulate it by the proper combination of resistors, capacitors and active devices, has only delayed the solution to the miniaturized inductance problem. (Reference to some of these techniques will be made in the review of literature.)

B. Statement of the problem.

The purposes of this investigation are to: (1) adapt the Linvill Lumped Model to the unsymmetrical junction diode thereby relating the physical make-up and internal properties of the device to the model, (2) attempt to optimize the parameter relationship and thus the model in terms of the inductance property, (3) obtain a small-signal equivalent circuit by relating the lumped model parameters to conventional (R,L,C) circuit parameters, and (4) to verify this equivalent circuit through a comparison of theoretical and experimental results.

C. Significance of the study.

Different investigators have observed the inductive behavior of certain unsymmetrically doped diodes at high current densities. The theory of operation and the theoretical derivation of an equivalent circuit from the differential equations of p-n junction theory, lead to long and complicated calculations. Previous attempts have included simplifying assumptions such as equal carrier mobilities, constant fields, and equal doping of the p and n regions. These

restrictions obviously complicate any comparison with experiment. A complete theoretical treatment of this inductive behavior is not known. An insight into various ways of improving the inductive behavior should be gained by relating the observed inductance to the structural make-up and internal physical properties.

D. Reasons for the investigation.

An interest in integrated electronics led to the author's interest in the inductance problem. The interest in integrated circuits stems partially from a belief similar to that of Dr. G. E. Moore, Director, Research and Development Laboratories of Fairchild Semiconductor, when he stated, "The future of integrated electronics is the future of electronics itself. The advantages of integration will bring about a proliferation of electronics, pushing this science into many new areas" (Moore 1965).

CHAPTER II

REVIEW OF THE LITERATURE

A. Active network and hybrid approach.

Research for the development of suitable inductors for microelectronics has taken many different paths. Alternate solutions to the inductance problem have been investigated whereby no attempt was made to develop an actual inductor. Dill (1961) and Khambata (1963) state that large inductance may be obtained from a transistor in combination with an RC phase-shift network. This is the impedance-inversion principle that is well known in electronic circuitry. Transistor circuits of this type have a low Q^* , usually less than unity, due to loading effects. Stone and Warner (1961) and Etter and Wilson (1962) treat the inductive properties of the field-effect tetrode device. Here the tetrode transistor is biased such that impedance inversion is obtained. Although reasonable inductance values are obtained, e.g., 0.55 mh at 422 Kc and 6 μ h at 14 Mc, the temperature stability of the device is not suitable for most circuit applications. Dill (1962) and Dutta Roy (1963) report on the inductive behavior of an "inductive" transistor. This device is an alloy transistor operating in the α -cutoff region. It is shown that a Q slightly greater than unity and inductance values in the mh range can be obtained over a limited frequency

* Q is a figure-of-merit factor defined as 2π times the ratio of the maximum energy stored to the energy dissipated per cycle in a circuit or component.

range. Dutta Roy (1964) obtains a Q of 70 at 200 Kc with an inductance of 0.7 mh by the compound connection of two transistors in a modified version of the inductive transistor circuit but gives no theoretical analysis. However, Dutta Roy obtains oscillations in the range 70 Kc to 230 Kc by shunting the circuit with a suitable capacitor. Limited frequency range and severe temperature instability are the main shortcomings of this inductance approach. Dill (1962) reports on the use of avalanche multiplication to increase the Q of the inductive transistor. A band pass amplifier with a Q of 50 is demonstrated but with limited frequency range and temperature stability. Dill (1962) also studied an inductive effect obtained from a unijunction transistor. Drift of Q and resonant frequency with temperature make this approach undesirable for microminiaturized circuits.

Each of the above-discussed active-device inductance circuits is some form of impedance converter and is not suitable for resonance or tuned-circuit applications. The poles of these networks are not confined to the left-half of the s -plane and, in effect, frequency selectivity is obtained only by operating on the verge of self oscillation. In contrast to passive networks, Q is easy to obtain but very difficult to maintain at a constant value. These "inductors" have to be either external to an integrated circuit package or installed within one of the taller of the TO-5* transistor packages. Recent reports (Warner

* The TO-5 standard designation refers to a package or "can" approximately $1/3$ inch in diameter and $1/4$ inch in height.

and Fordemwalt, 1965) of small toroidal coils made of powdered iron or special ferrites appear more favorable than the above techniques if the hybrid circuit approach is to be used. These small toroidal coils are comparable to TO-5 cans in size and have inductance and Q values compatible to hybrid circuit applications. Warner and Fordemwalt list various core sizes with data ranging from $L = 40 \mu\text{h}$ and $Q = 70$ at 40 Kc, to $L = 10 \mu\text{h}$ and $Q = 220$ at 100 Mc.

B. Thin-film approach.

Considerable effort has been expended to develop inductance in a thin-film process. Warner and Fordemwalt (1965) report on a flat spiral inductor with $L = 3.91 \mu\text{h}$, $Q = 35.1$ at 80 Mc. Limited results have been obtained by sequential deposition of thin-film conductors, insulators and magnetically oriented films (Schlaback and Rider, 1963). Schlaback and Rider give another technique involving the deposition of a highly conductive film in the form of a Archimedean spiral using alternate depositions of these properly oriented multilayer spirals with insulators. Khambata (1963) reports that thin-film, deposited ferrite, inductors have been made variable by varying the permeability of the ferrite core through application of a d-c magnetic field. The properties of these deposited inductors depend upon the physical configuration chosen, i.e., number of turns, radius and width of lines, and the thickness of conductor used. Large inductance necessitates bulky physical size as compared to other integrated circuit components. Dielectric properties of insulation and substrate also hamper the development of good deposited inductors. Therefore, until improved results are obtained, it seems likely that any necessary inductance

will have to be placed external to the thin-film region by using the hybrid technique.

C. Monolithic approach.

The monolithic approach to the inductance solution has been concentrated on a device once considered of rather secondary importance with respect to the transistor, i.e., the junction diode. Shockley's (1959) early work considered the diffusion admittance of the p-n junction as a function of frequency. The treatment, however, was restricted to low injection levels and considered only minority carrier flow. This resulted in an imaginary admittance term which was attributed to diffusion capacitance. Kanai (1954), Misawa (1957), and Armstrong (1957) observed inductive effects in p-n diodes at high current levels. Although several theories were introduced to explain the inductance properties, Kanai (1955) and Yamaguchi (1956) were among the first to attribute them to conductivity modulation*. Kanai (1955), Firle and Hayes (1959), and Ladany (1960) have all analyzed the inductive reactance under small signal excitation. Firle and Hayes also considered the diode impedance as a function of forward bias current. Ladany and others (Nishizawa and Watanabe, 1960; Nordman and Greiner, 1963) have suggested special diode geometries to enhance this conductivity modulation and have termed these diodes, "inductance diodes." Armstrong (1957) and Vannoy (1964) have studied the pulse response of the p-n junction after attributing the inductive phenomenon to conductivity modulation. Armstrong used a change in bias level

* See Chapter III for discussion of conductivity modulation.

approximating a current step, Vannoy used a voltage step. Misawa (1957) and Ko (1961) have made mathematical justification of the inductive properties. Nishizawa and Watanoba (1960) describe the theory and preparation of a high-Q inductance diode. Limited success is reported by using a $p^+n p n^+$ structure to obtain negative resistance in series with the inductive property, thereby improving the Q. The inductance of this device was in the millihenry range at frequencies up to 1 Mc. The highest stable Q was 30. Ladany and Kearney (1961) used a double-base diode, a simpler version of the Nishizawa and Watanaba device, to obtain a Q approaching 1000 and $L = 2$ mh in a frequency rejection filter operating near 35 Kc. Schuller and Gärtner (1960) discuss a diffused-base transistor with open-circuit base connection. By operating in the avalanche multiplication region, the device behaves as an inductive negative-resistance diode. A coilless L-C circuit was constructed with resulting resonance at 1.3 Mc. Development of these inductance negative-resistance devices appears promising if research can reduce the avalanche noise and solve the temperature instability problem. These devices can be fabricated in a monolithic functional block with predicted performance as soon as the inductance negative-resistance effect is fully understood. Vannoy (1964) suggests that it may be possible to use a tunnel diode in series with the inductance diode in order to improve and control the Q. Dill (1961) previously reported poor results with this method due to the voltage-biased tunnel diode. The combination of a voltage-stable negative-resistance device and a temperature-sensitive inductance diode produces an extremely unstable d-c operating point.

D. Summary.

In summary, a review of the research that has been done in this area shows that values of realizable inductance, Q , and operating frequency all lie in the range of major circuit interest. However, many problems and questions remain unanswered. How can these devices be temperature stabilized? How can unwanted oscillations be prevented in those devices that use a negative resistance to increase the Q ? How can the avalanche noise be reduced in those devices operating in the avalanche multiplication region? What are the optimized geometries necessary to enhance the inductance property? What semiconductor properties can be optimized to improve this inductance?

After consideration of the previous work, it is the author's opinion that the inductance diode is the best approach to follow in obtaining an inductor compatible with monolithic circuits. The first steps to be taken must be toward improving the Q and increasing the inductance values. The remainder of this thesis will be devoted to the last two questions proposed above in an attempt at improving these properties.

CHAPTER III

INDUCTANCE DIODES

A. Theory.

A p-n junction diode can be shown to have a reactance that is a function of bias current (Firle and Hayes, 1959). At zero bias, this reactance is capacitive and is a result of the barrier space-charge capacitance. As the bias is increased in the forward direction, the diode may behave as if it contained inductive elements. This phenomenon has been attributed to delayed conductivity modulation (Kanai, 1955; Yamaguchi, 1956). The basic requirement for the existence of conductivity modulation and thus inductance in a junction diode is that there be a non-negligible electric field in the base (lightly doped) region. A second requirement is that enough minority carriers be injected to modulate the base conductivity.

When a difference of potential is applied across a diode consisting of a highly doped p region and a lightly doped n region, it is partitioned between the junction and the base. Since the p region is heavily doped, the voltage drop across the p material is negligible. The voltage drop across the base produces a field in this region and thus a drift current given by $J = \sigma \mathcal{E}$. This conductivity σ is not a constant but depends on the carrier concentration ($\sigma = Ne\mu$). It is thus controlled in magnitude by the voltage across the barrier and the injection mechanism. Assume that a step voltage is applied across the diode; then a current is injected into the base and the conductivity increases. This

increase in conductivity does not occur immediately because the carriers must spread throughout the base by diffusion. For a wide-base, symmetrically doped diode, the time required for the diffusion process would be equal to the lifetime of the carriers,

$$\tau_p = \frac{L_p^2}{D_p} \quad (1)$$

L_p is the hole diffusion length and D_p is the corresponding diffusion constant. For lightly doped (nearly intrinsic) materials, (1) can be written

$$\Delta \tau \approx \frac{d^2}{2 D'} \quad (2)$$

L_p is replaced with d where $d \leq L_p$ to include base widths less than the diffusion length. For intrinsic material, the effective diffusion constant is $D' = D_p D_n / (D_p + D_n)$. Correspondingly, the current increases from a negligible value to a value V/R_b where R_b is the base resistance and V is the voltage across the base. Writing this change in current as $\Delta I = V/R_b$ and dividing by (2) results in

$$\frac{\Delta I}{\Delta \tau} = \frac{V}{R_b} \frac{2 D'}{d^2} \quad (3)$$

If inductance is defined by means of

$$V = L \frac{di}{d\tau} \quad (4)$$

where v and i are the instantaneous voltage and current respectively,

inspection of (3) results in the following estimate for the inductance of the base region

$$L \approx \frac{R_b d^2}{2 D'} \quad (5)$$

The resistance R_b is proportional to $\frac{d}{\sigma A}$ (where A is the diode cross section) and is a function of V . Although this is a simplified picture neglecting other sources of current in the diode, the important result is that under certain conditions the phase of the applied voltage leads that of the base current by 90° . This indicates that there is an inductive effect.

A more rigorous mathematical analysis indicates that the inductance property is greatest at zero bias (Ladany, 1960). It is, however, in series with the reactance property of the diffusion capacitance and is overshadowed by the capacitive term. As the bias is increased, the inductive reactance decreases, but the capacitive reactance decreases even faster. At some bias value, the two reactances cancel and the diode is purely resistive. This bias level is dependant upon the physical make-up of the diode. Firlle and Hayes (1959) experimently determined that 5 ma is a typical value for silicon abrupt-junction diodes of approximately 1 mm^2 junction area.

B. Description of inductance diodes.

Two basic requirements for the existence of inductance in a forward-biased junction diode were previously given. These were

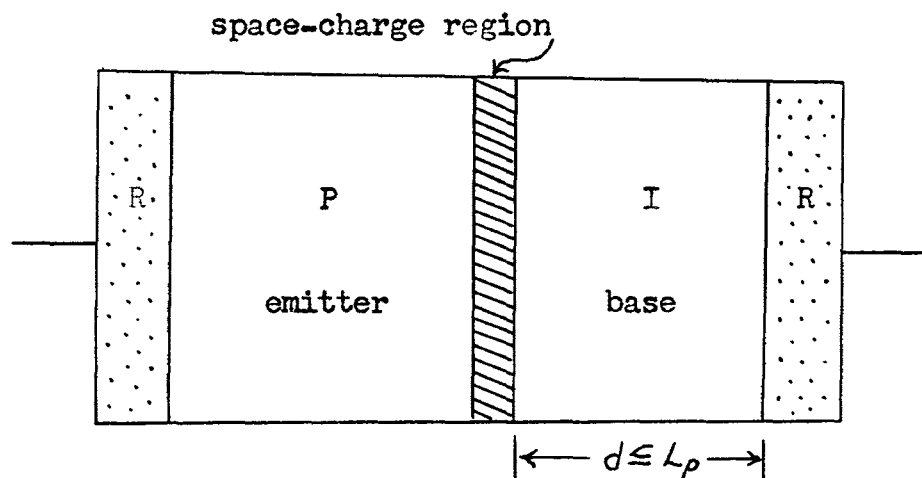


Figure 1. The narrow-base PIR diode

an electric field in the base region and enough minority carrier injection to modulate the base conductivity. Figure 1 is a schematic diagram of a narrow-base diode suggested by Ladany (1960). Ladany simplified his analysis by eliminating volume recombination in the quasi-neutral base region. This is accomplished by the narrow-base restriction of the base width equal to or less than the hole diffusion length. The base region is indicated by the I and is very nearly intrinsic. This intrinsic base permits the neglecting of the electric field when determining carrier concentration. This does not mean that no field currents are flowing. A previous requirement was that a field must be present in the base. However, these field currents do not influence the carrier distribution. They are due to the injection of charged

carriers and neutrality is still approximately satisfied. The P region is an emitter so heavily doped with acceptors that no voltage drop need be considered here. The R regions are described as "infinite recombination velocity" contacts. These noninjecting ohmic contacts have a negligible impedance. They also maintain equilibrium concentration under all conditions by serving as a nearly perfect sink or source of excess carriers. This behavior is approached in semiconductor contacts by using a lead or tin alloyed contact. Figure 2 is a diagram of a PIR diode as shown by Dill (1961). This "wide-base" diode is a better representation of the normal unsymmetrical diode. The unmodulated base region adds nothing to the inductance property and reduces the device Q by adding series resistance.

A different inductance diode has been suggested by Nordman and Greiner (1963). Shown in Figure 3, it is symmetrical in that the doping level of the P region is equal to the doping level of the N region. The junctions are abrupt and doping densities are sufficient to neglect any voltage drop in the doped regions. Each of the doped regions serves as a carrier injection source in an effort to double the effects of conductivity modulation.

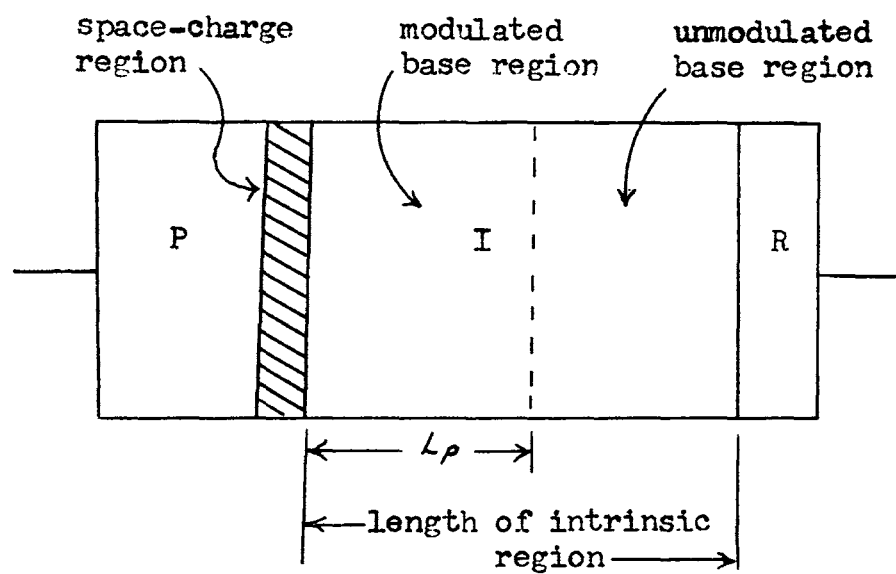


Figure 2. A wide-base PIR diode.

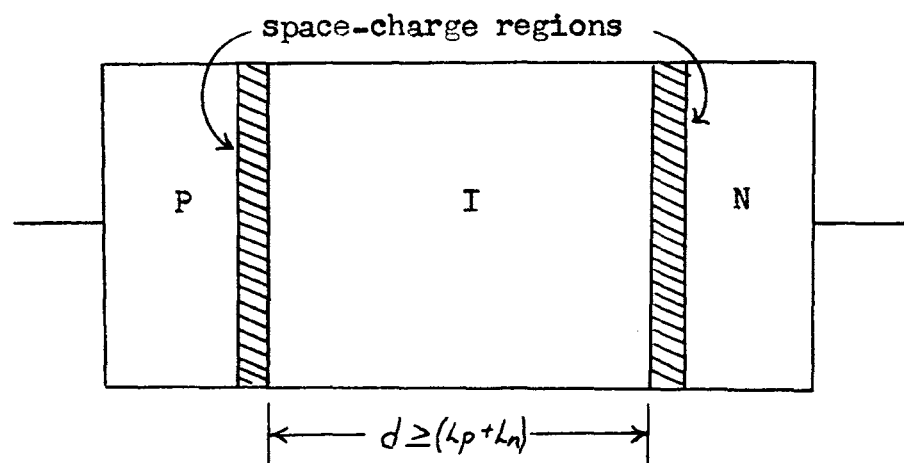


Figure 3. A PIN diode

CHAPTER IV

A DISCUSSION OF MODELS

In considering an active device such as a vacuum tube or any of the solid state devices, it is often found that the physical behavior, for certain defined operating conditions, can be represented by a combination of ideal elements. This representation is called an equivalent circuit or model. The model is a mathematical entity and is always distinct from the physical device. It is thus an approximation and is never actually equivalent to the device it represents. The degree of approximation is directly dependent upon the preciseness used by the analyst in defining the model properties or variables and to the degree that laws of physics are followed. A compromise must be reached between simplicity and accuracy. This compromise is usually influenced by the intended application of the device and model. For example, the simple piecewise-linear equivalent circuit used for transistors is sufficient for some waveshaping and switching applications. The more detailed hybrid-parameter equivalent circuit is preferred if the model is to represent the transistor in the analysis of a small-signal audio amplifier.

Models which identify relationships between the external variables of a device without explicitly considering the internal physical processes are called functional models. Models which relate the external behavior to the internal physical processes are called physical models. Functional models are most useful to the electronic circuit designer while the physical model is

of more importance in the design and understanding of the device. The field of solid state electronics requires much overlap of these two model concepts since in order to use a device in the optimum manner, the circuit designer must have reasonable familiarity with the physics of that device.

Although the model used in this thesis might be termed a physical model or even a model of a process, it can be used as a functional model. It should be kept in mind, however, that the author's aim is to relate the physical make-up and internal properties of the device to the model, hopefully in such a manner as to better explain and to optimize the inductive behavior of unsymmetrical diodes. Usefulness as a functional model is improved if the final equivalent circuit is used with the parameter constants (R , L , C) rather than the notation and relationships as developed by Linvill (Linvill 1958).

CHAPTER V

FINITE DIFFERENCE EQUATIONS AND THE LINVILL MODEL

Linvill (1958; 1963) has introduced a lumped model representation for the finite difference equations describing the current flow through a bulk semiconductor region. Consider an n-type semiconductor bulk as shown in Figure 4. The carrier flow is assumed to be one-dimensional. This bulk region can be subdivided into equal volume elements of length Δx and cross section area A . Only the excess carrier densities p_i and n_i , and the equilibrium carrier densities p_n and $n_n = p_n + N_d$ at the centers of the volumes will be considered. N_d is the ionized impurity density and is constant.

The differential equations for the hole- and electron-flow through an n-type bulk semiconductor are given by Linvill and Gibbons (1961) to be

$$\frac{\partial p}{\partial t} = - \frac{1}{e} \frac{\partial j_p}{\partial x} - \frac{p - p_n}{\tau_p} \quad (6)$$

$$\frac{\partial n}{\partial t} = \frac{1}{e} \frac{\partial j_n}{\partial x} - \frac{p - p_n}{\tau_p} \quad (7)$$

These are known as the continuity equations where e is the magnitude of the unit electronic charge, p is the mean density of holes, n is the mean density of electrons and j with appropriate subscript is the current density. These equations state that any change in

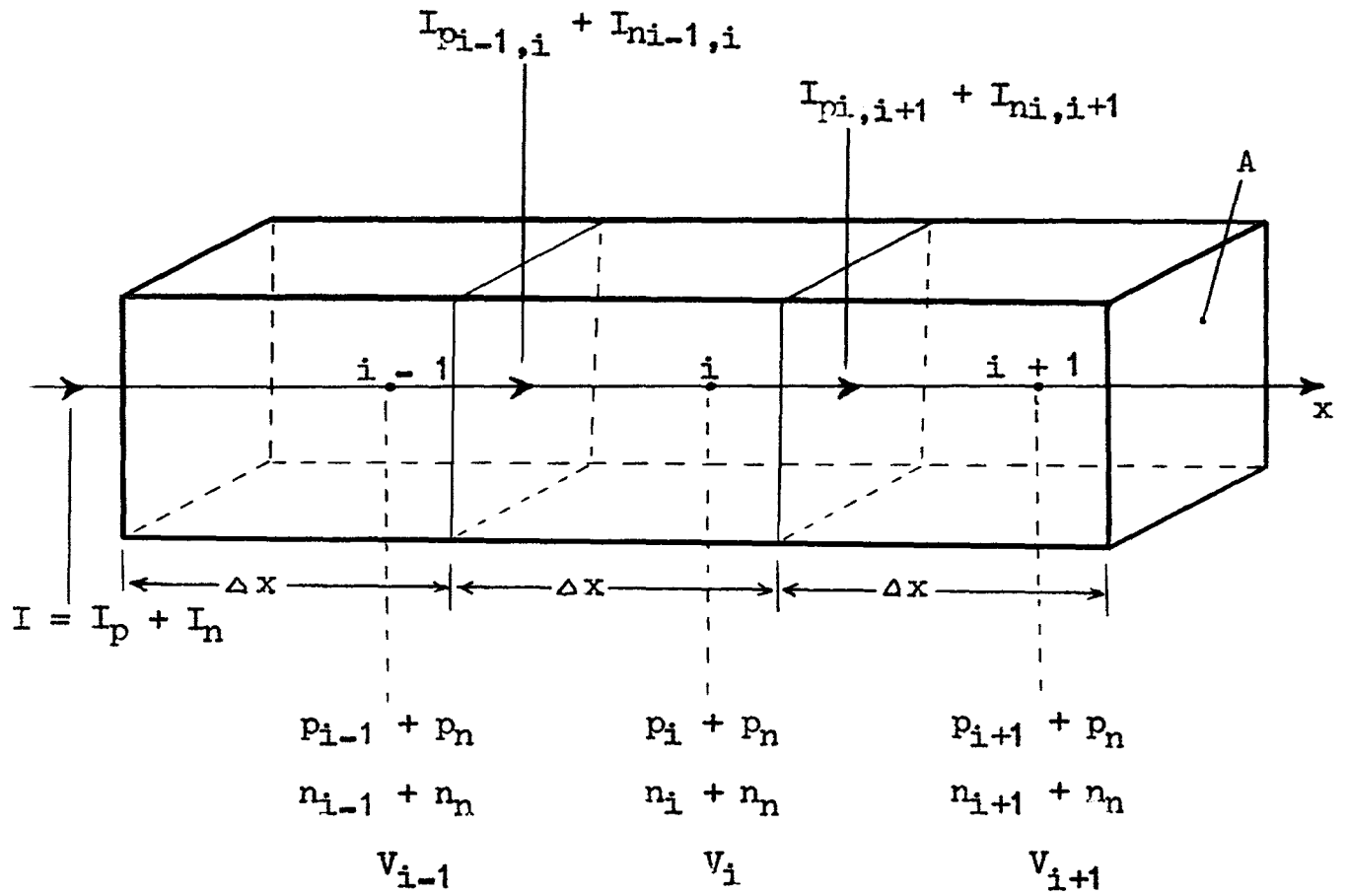


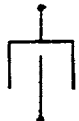

Figure 4. Semiconductor bulk region with one-dimensional carrier flow.

population density of holes in any region must be in accordance with hole flow to and from the region and generation-recombination inside the region. Using the assumption that the carrier generation and recombination depends only on the excess densities of the minority carriers p_i in the center of the volume elements, the continuity equations can be transformed into the finite difference equations

$$eA\Delta x \frac{\partial p_i}{\partial t} = -eA\Delta x \frac{p_i}{\tau_p} - \left(\frac{A j_{p,i,i+1} - A j_{p,i,i-1}}{\Delta x} \right) \Delta x \quad (8)$$

$$eA\Delta x \frac{\partial n_i}{\partial t} = -eA\Delta x \frac{p_i}{\tau_p} - \left(\frac{A j_{n,i,i+1} - A j_{n,i,i-1}}{\Delta x} \right) \Delta x \quad (9)$$

where $A j_{p,i,i+1} = I_{p,i,i+1}$ and $A j_{n,i,i+1} = I_{n,i,i+1}$ are the hole and electron currents between the centers of two adjacent volume elements. Using the elements of the lumped model as introduced by Linvill (1958),

storance	combinance
$S = eA\Delta x$ 	$H_c = \frac{eA\Delta x}{\tau_p}$ 

equations (8) and (9) become

$$S \frac{\partial p_i}{\partial x} = -H_c p_i + I_{p_{i-1}, i} - I_{p_{i, i+1}} \quad (10)$$

$$S \frac{\partial n_i}{\partial x} = -H_c p_i + I_{n_{i, i+1}} - I_{n_{i-1}, i} \quad (11)$$

The hole and electron currents of two adjacent volume elements are related to the carrier concentrations and the voltage drop between the centers of the adjacent elements. These currents may be written as the sum of a drift component given in differential form by

$$\begin{aligned} i_p &= e \mu_p A p E \\ i_n &= e \mu_n A n E \end{aligned} \quad (12)$$

and a diffusion component given by

$$\begin{aligned} i_p &= -e A D_p \frac{\partial p}{\partial x} \\ i_n &= e A D_n \frac{\partial n}{\partial x} \end{aligned} \quad (13)$$





where μ_p and μ_n are the carrier mobilities and D_p and D_n are the diffusion constants of the holes and electrons respectively.

Addition of components and conversion to difference form gives
for elements $i, i+1$

$$I_{p_i, i+1} = -eA\mu_p \left(p_n + \frac{p_i + p_{i+1}}{2} \right) \left(\frac{V_{i+1} - V_i}{\Delta x} \right) - eAD_p \left(\frac{p_{i+1} - p_i}{\Delta x} \right) \quad (14)$$

$$I_{n_i, i+1} = -eA\mu_n \left(n_n + \frac{n_i + n_{i+1}}{2} \right) \left(\frac{V_{i+1} - V_i}{\Delta x} \right) - eAD_n \left(\frac{n_{i+1} - n_i}{\Delta x} \right) \quad (15)$$

Again using Linvill's (1958) lumped model elements as defined by

<p>hole mobillance</p> $M_p = \frac{eA\mu_p}{\Delta x}$ 	<p>electron mobillance</p> $M_n = \frac{eA\mu_n}{\Delta x}$ 
<p>hole diffusance</p> $H_p = \frac{eAD_p}{\Delta x}$ 	<p>electron diffusance</p> $H_n = \frac{eAD_n}{\Delta x}$ 

Equations (14) and (15) can be written as

$$I_{p_i, i+1} = -M_p \left(\rho_n + \frac{\rho_i + \rho_{i+1}}{2} \right) (V_{i+1} - V_i) - H_p (\rho_{i+1} - \rho_i) \quad (16)$$

$$I_{n_i, i+1} = -M_n \left(n_n + \frac{n_i + n_{i+1}}{2} \right) (V_{i+1} - V_i) + H_n (n_{i+1} - n_i) \quad (17)$$

A lumped model for volume element i is given in Figure 5. The values of the mobilities and diffusivities are shown doubled. This has been done because they account for the distance from the center of element i to the adjacent element, e.g., $\Delta x/2$. The model shown is an actual physical model of the semiconductor in which the accuracy depends only on the element width Δx and the assumption that carrier generation and recombination depend only on minority carrier excess density. With this model and equations (10), (11), (16) and (17), the transport mechanisms can be related to the semiconductor geometry and the physical constants.

Outside the space-charge region in a semiconductor, Poisson's equation can be replaced by a quasi-neutrality condition known as space-charge neutrality. This is the approximation that any introduction of minority carriers is immediately accompanied by flow of majority carriers such that neutrality is maintained.

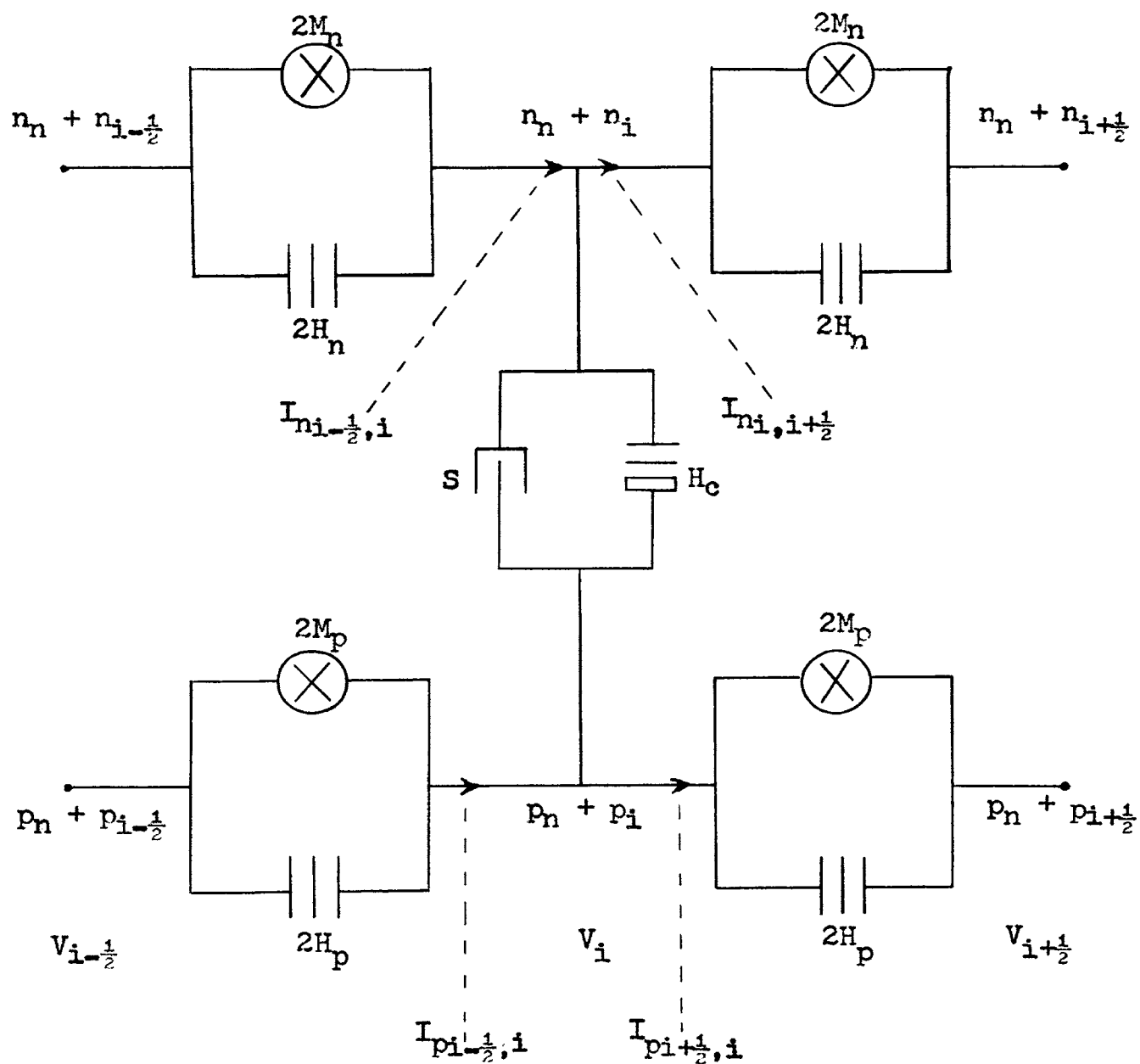


Figure 5. Lumped model representation of carrier flow through a semiconductor volume element i .

Space charge neutrality implies that

$$\begin{aligned}n_n &= p_n + N_d \\ n_i &= p_i\end{aligned}\tag{18}$$

Equations (18) relate the majority and minority carrier concentrations. They can be used to eliminate one type of these concentrations in the continuity equations (10) and (11) and current equations (16) and (17).

CHAPTER VI

ANALYSIS OF AN UNSYMMETRICALLY DOPED P-N DIODE

A. Lumped model.

The finite difference equations and the lumped model of Chapter V can be applied to semiconductor diodes. Consider the diode shown in Figure 6. The junction is abrupt and the p region is assumed to be so heavily doped that its influence can be neglected in comparison to the lightly doped n region.

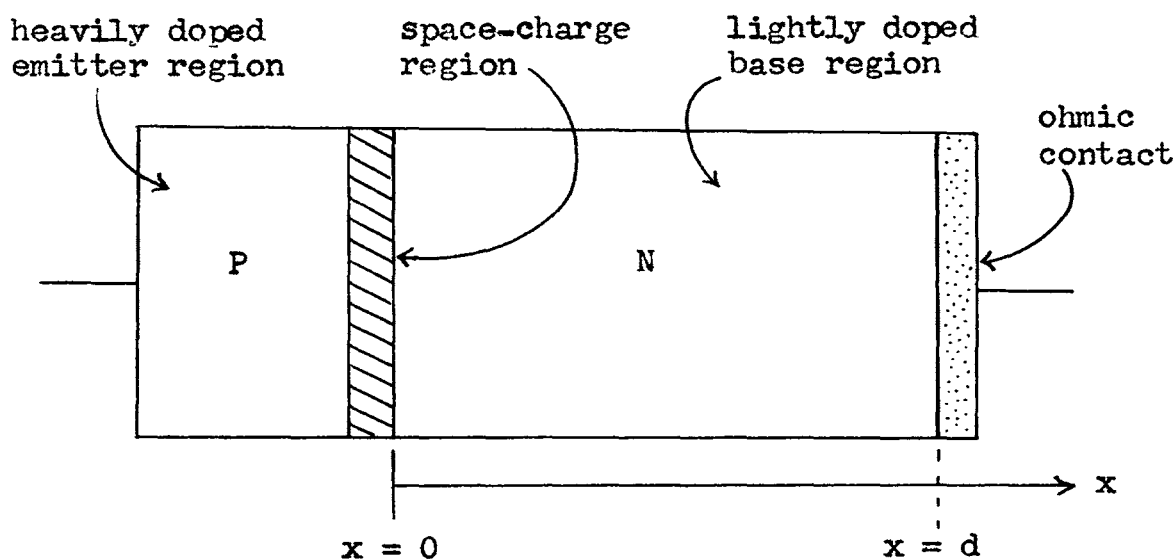


Figure 6. Unsymmetrically doped junction diode.

Linvill and Gibbons (1961) have shown that the space-charge junction region can be represented by the model given in Figure 7. The equations are referred to as the "laws of the junction." V_J is the voltage drop across the space-charge region. n_J and p_J are the excess carrier densities at the boundary of the junction. The laws of the junction relate this voltage to the concentration of excess minority carriers at the boundaries between the space-charge

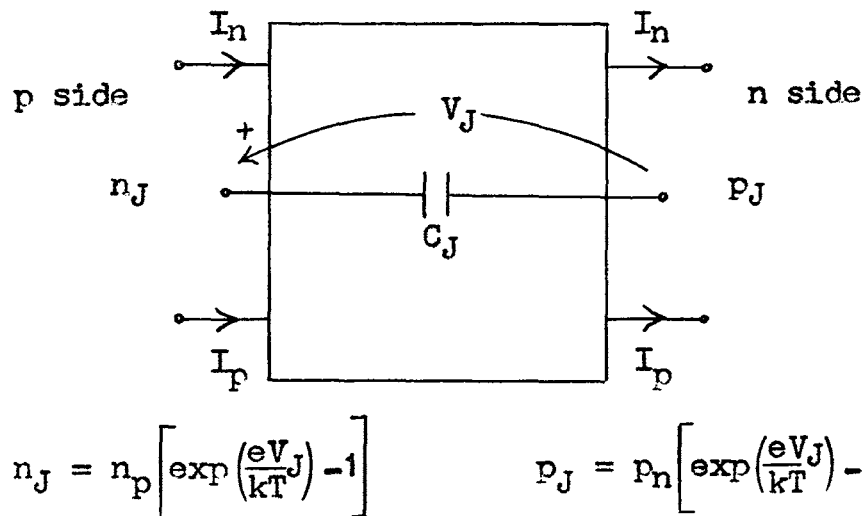


Figure 7. Model of a p-n junction.

region and the bulk regions. C_J is the space-charge capacitance and will be neglected in this analysis. The neglecting of C_J is justified by the fact that the magnitude of the diffusion capacitance is much larger than C_J if the diode is operated at normal to high forward current densities. Diffusion capacitance is implicitly accounted for in the storage element. It is further assumed that only hole current $I = I_p$ flows across the boundary between the p and n regions. This assumption and the neglecting of C_J gives a boundary condition for the electron current in the lightly doped n region

$$I_n (x=0) = 0 \quad (19)$$

Another boundary condition, vanishing excess carrier concentration

$$P_i (x = d) = 0 \quad (20)$$

can be obtained if the ohmic metal-semiconductor contact is assumed to be an infinite recombination velocity region.

The outlined assumptions and boundary condition can now be incorporated with the lumped model of Figure 5 and the junction model of Figure 7 to give a lumped model of the unsymmetrical diode. This single section lumped model is shown in Figure 8. The i notation is dropped in the interest of simplicity as only one element is considered here. This simple lumped model describes the diffusion mechanism and the conductivity modulation in the n-type base region. Using the results of Chapter V, the following equations apply to the model,

$$I_{n,2} = -2M_n \left(\rho_n + N_d + \frac{\rho_1 + \rho_2}{2} \right) (V_2 - V_1) + 2H_n (\rho_2 - \rho_1) \quad (21)$$

$$I_{n,3} = -2M_n \left(\rho_n + N_d + \frac{\rho_2 + \rho_3}{2} \right) (V_3 - V_2) + 2H_n (\rho_3 - \rho_2) \quad (22)$$

$$I_{p,2} = -2M_p \left(\rho_n + \frac{\rho_1 + \rho_2}{2} \right) (V_2 - V_1) - 2H_p (\rho_2 - \rho_1) \quad (23)$$

$$I_{p,3} = -2M_p \left(\rho_n + \frac{\rho_2 + \rho_3}{2} \right) (V_3 - V_2) - 2H_p (\rho_3 - \rho_2) \quad (24)$$

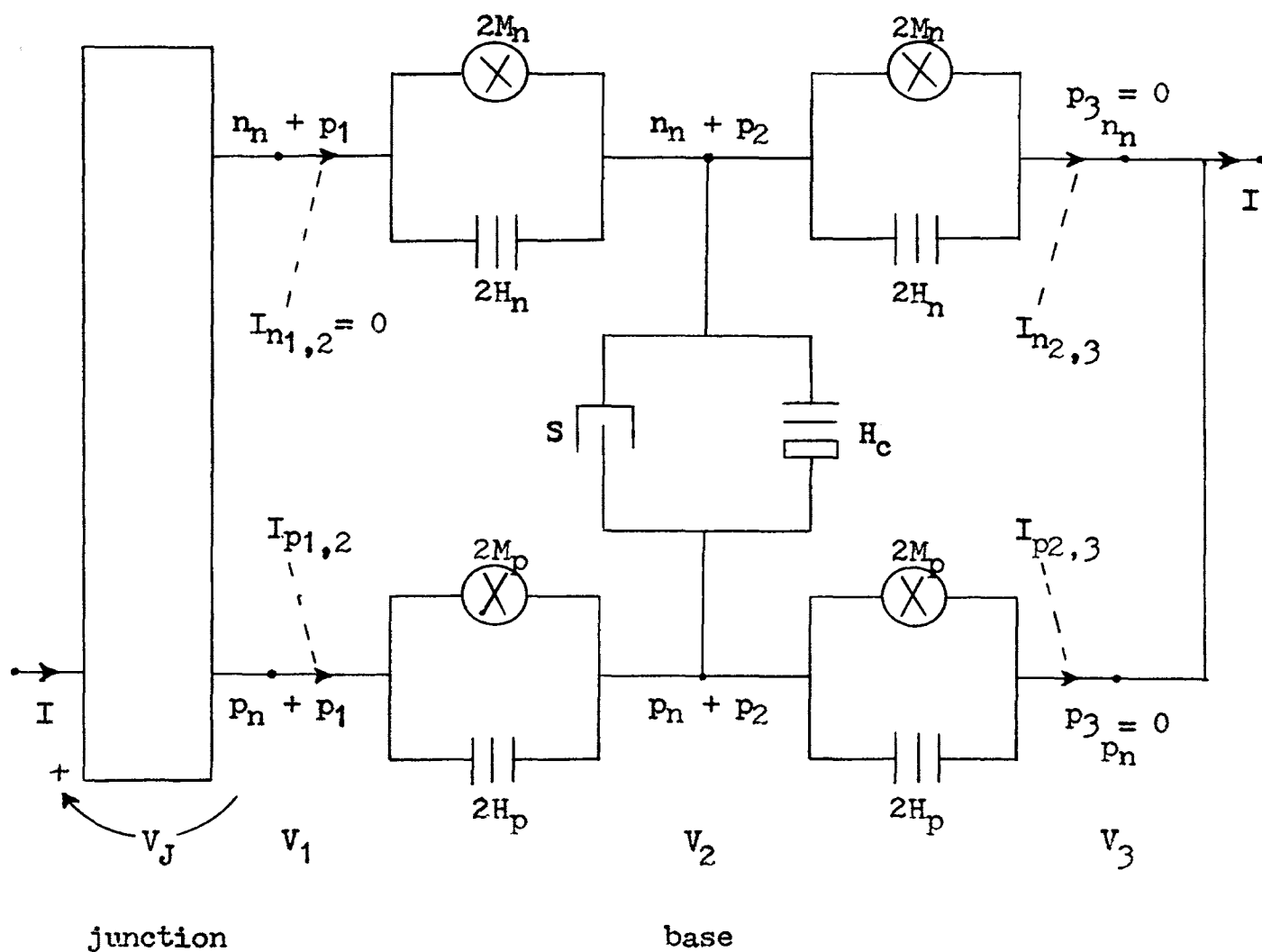


Figure 8. Single-section lumped model of unsymmetrically doped junction diode.

$$S \frac{d\rho_2}{dt} = -H_c \rho_2 + I_{\rho_1,2} - I_{\rho_2,3} \quad (25)$$

$$I = I_{n_1,2} + I_{\rho_1,2} = I_{n_2,3} + I_{\rho_2,3} \quad (26)$$

Examination of the six equations (21) - (26) reveals ten unknowns*. However equation (26) is actually two equations and the boundary conditions (19) and (20) can be used to eliminate two unknowns. This leaves eight unknowns and seven equations. By elimination of all other unknowns, except I, a nonlinear first-order differential equation with respect to time is obtained for the volume concentration ρ_2 .

$$\frac{S}{2H_p} \frac{\partial \rho_2}{\partial t} = -\frac{H_c}{2H_p} \rho_2 + \frac{\frac{I}{2H_p} \left[N_d + \rho_n + \frac{\rho_2}{2} \right] - \rho_2 \left[N_d + 2\rho_n + \rho_2 \right]}{\frac{M_p}{M_n} \left[\rho_n + \frac{\rho_2}{2} \right] + \left[N_d + \rho_n + \frac{\rho_2}{2} \right]} \quad (27)$$

The solution of this equation for a small perturbation signal results in a small signal equivalent circuit.

B. Small signal equivalent circuit.

At high injection levels ($\rho_2 \gg \rho_n, N_d$), equation (27) reduces to

$$\left[\frac{S}{H_p} \frac{d\rho_2}{dt} + \frac{H_c}{H_p} \rho_2 \right] \left[1 + \frac{M_p}{M_n} \right] + 4\rho_2 = \frac{I}{H_p} \quad (28)$$

* N_d , ρ_n and the model elements can be determined from the diode dimensions and physical constants.

If a small a-c current is superimposed on the existing forward bias current, perturbations of the excess carrier densities and the diode voltages will appear.

Let $p_2(t)$ be equal to $p_2 \exp(j\omega t)$ where the superimposed current is $I \exp(j\omega t)$. Equation (28) becomes

$$\bar{p}_2 = \frac{\bar{I}}{H_p} \frac{1}{\left[4 + \frac{H_c}{H_p} \left(1 + \frac{M_p}{M_n}\right)\right] \left[1 + j\omega \frac{\frac{S}{H_p} \left(1 + \frac{M_p}{M_n}\right)}{4 + \frac{H_c}{H_p} \left(1 + \frac{M_p}{M_n}\right)}\right]} \quad (29)$$

where the quantities \bar{p}_2 and \bar{I} are phasors. From the difference equations (21) - (26)

$$p_1 - p_2 = \frac{I}{2H_p} \left[\frac{N_d + p_n + \frac{p_1 + p_2}{2}}{N_d + 2p_n + p_1 + p_2} \right] \quad (30)$$

For high injection levels, ($p_2 \gg p_n, N_d$), equation (30) reduces to

$$p_1 - p_2 = \frac{I}{4H_p} \quad (31)$$

Rewriting (31) in terms of small signal components

$$\bar{\rho}_1 = \frac{\bar{I}}{4 H_p} + \bar{\rho}_2 \quad (32)$$

Using equation (29) in equation (32) results in

$$\bar{\rho}_1 = \frac{\bar{I}}{4 H_p} \left\{ 1 + \frac{1}{\left[1 + \frac{H_c}{4 H_p} \left(1 + \frac{M_p}{M_n} \right) \right] \left[1 + j \omega \frac{\frac{S}{4 H_p} \left(1 + \frac{M_p}{M_n} \right)}{1 + \frac{H_c}{4 H_p} \left(1 + \frac{M_p}{M_n} \right)} \right]} \right\} \quad (33)$$

The exponential term of the law of the junction can be expanded in a power series

$$\exp \left(\frac{e V_J}{k T} \right) = 1 + \frac{e V_J}{k T} + \left(\frac{e V_J}{k T} \right)^2 \frac{1}{2!} + \dots$$

Retaining the first two terms, the law of the junction for small signal excitation becomes

$$\bar{\rho}_1 = \rho_1 \frac{e \bar{V}_J}{k T} \quad (34)$$

where \bar{V}_J is a phasor quantity.

Equating (33) and (34)

$$\rho_i \frac{e \bar{V}_J}{kT} = \frac{\bar{I}}{4 H_p} \left[1 + \frac{1}{1 + \frac{H_c}{4 H_p} \left(1 + \frac{M_p}{M_n} \right) + j\omega \frac{S}{4 H_p} \left(1 + \frac{M_p}{M_n} \right)} \right] \quad (35)$$

Defining the small signal junction impedance as

$$\bar{Z}_J = \frac{\bar{V}_J}{\bar{I}} \quad (36)$$

and solving for \bar{Z} from (35)

$$\bar{Z} = \left[\frac{kT}{e} \right] \left[\frac{1}{4 H_p \rho_i} \frac{2 + \frac{H_c}{4 H_p} \left(1 + \frac{M_p}{M_n} \right)}{1 + \frac{H_c}{4 H_p} \left(1 + \frac{M_p}{M_n} \right) + j\omega \frac{S}{4 H_p} \left(1 + \frac{M_p}{M_n} \right)} \right] \cdot \quad (37)$$

$$\left[\frac{1 + j\omega \frac{S}{4 H_p} \left(1 + \frac{M_p}{M_n} \right)}{2 + \frac{H_c}{4 H_p} \left(1 + \frac{M_p}{M_n} \right)} \right]$$

$$\left[\frac{1 + j\omega \frac{S}{4 H_p} \left(1 + \frac{M_p}{M_n} \right)}{1 + \frac{H_c}{4 H_p} \left(1 + \frac{M_p}{M_n} \right)} \right]$$

Examination of the second term in brackets by a dimensional analysis shows that it is the reciprocal of a current. As no time variation

is included, it must be a d-c current.

$$I_{dc} = 4 H_p P_1 \left[\frac{1 + \frac{H_c}{4 H_p} \left(1 + \frac{M_p}{M_n} \right)}{2 + \frac{H_c}{4 H_p} \left(1 + \frac{M_p}{M_n} \right)} \right] \quad (38)$$

Replacing p_1 by

$$P_1 = P_n \left[\exp \left(\frac{e V_J}{k T} \right) - 1 \right] \quad (39)$$

$$I_{dc} = 4 H_p P_n \left[\frac{1 + \frac{H_c}{4 H_p} \left(1 + \frac{M_p}{M_n} \right)}{2 + \frac{H_c}{4 H_p} \left(1 + \frac{M_p}{M_n} \right)} \right] \left[\exp \left(\frac{e V_J}{k T} \right) - 1 \right] \quad (40)$$

This same expression for the d-c current through the space-charge region can be obtained directly from the difference equations (21) - (26) and the law of the junction (39).

The small signal junction impedance can now be written as

$$\bar{Z}_J = \left(\frac{k T}{e I_{dc}} \right) \left[\frac{1 + j\omega \frac{\frac{S}{4 H_p} \left(1 + \frac{M_p}{M_n} \right)}{2 + \frac{H_c}{4 H_p} \left(1 + \frac{M_p}{M_n} \right)}}{1 + j\omega \frac{\frac{S}{4 H_p} \left(1 + \frac{M_p}{M_n} \right)}{1 + \frac{H_c}{4 H_p} \left(1 + \frac{M_p}{M_n} \right)}} \right] \quad (41)$$

Equation (41) is of the form

$$\bar{Z} = a \frac{1 + j\omega\tau b}{1 + j\omega\tau} \quad (42)$$

and is the impedance of the phase lead network shown in Figure 9

where

$$\tau = R_1 C \quad b = \frac{R_2}{R_1 + R_2} \quad a = R_1 + R_2 \quad (43)$$

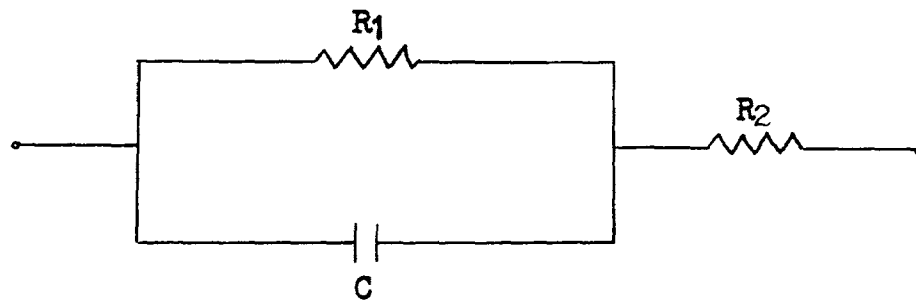


Figure 9. Phase lead network (small-signal equivalent circuit of unsymmetrical diode junction at high injection levels)

From (41), (42), and (43)

$$R_1 = \frac{kT}{e I_{dc}} \frac{1}{2 + \frac{H_c}{4 H_p} \left(1 + \frac{M_p}{M_n}\right)} \quad (44)$$

$$R_2 = \frac{kT}{eI_{dc}} \frac{1 + \frac{H_c}{4H_p} \left(1 + \frac{M_p}{M_n}\right)}{2 + \frac{H_c}{4H_p} \left(1 + \frac{M_p}{M_n}\right)} \quad (45)$$

$$C = \frac{eI_{dc}}{kT} \frac{S}{4H_p} \left(1 + \frac{M_p}{M_n}\right) \frac{2 + \frac{H_c}{4H_p} \left(1 + \frac{M_p}{M_n}\right)}{1 + \frac{H_c}{4H_p} \left(1 + \frac{M_p}{M_n}\right)} \quad (46)$$

The small signal impedance of the bulk region can now be found in a similar manner. An attempt to find the complete bulk impedance in one step leads to difficulties in that one portion of the bulk has a high injection level and the other part near $x = d$ has low injection. Using the condition of high injection levels, the boundary condition (19), and the difference equations (21) - (26), the voltage from $x = 0$ to $x = d/2$ is

$$\bar{V}_1 - \bar{V}_2 = \frac{kT}{e} \left[\frac{\bar{P}_1 P_2 - \bar{P}_2 P_1}{P_1 P_2} \right] \quad (47)$$

From equations (29), (38), (47), and the definition

$$\bar{Z}_{1,2} = \frac{\bar{V}_1 - \bar{V}_2}{\bar{I}} \quad (48)$$

The bulk impedance of the region $0 \leq x \leq d/2$ is

$$\bar{Z}_{1,2} = \frac{kT}{eI_{dc}} \left[\frac{j\omega \frac{S}{4H_p} \left(1 + \frac{M_p}{M_n}\right)}{2 + \frac{H_c}{4H_p} \left(1 + \frac{M_p}{M_n}\right)} \right. \\ \left. \frac{1 + j\omega \frac{S}{4H_p} \left(1 + \frac{M_p}{M_n}\right)}{1 + \frac{H_c}{4H_p} \left(1 + \frac{M_p}{M_n}\right)} \right] \quad (49)$$

Equation (49) is of the form

$$\bar{Z} = \frac{j\omega \tau a}{1 + j\omega \tau} \quad (50)$$

and represents the impedance of a RL network as shown in Figure 10

where

$$\tau = \frac{L}{R_3} \quad a = R_3 \quad (51)$$

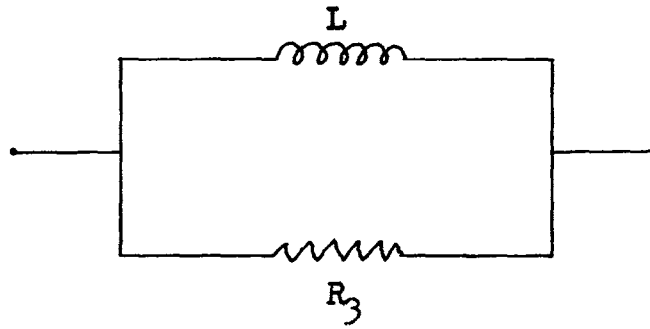


Figure 10. RL circuit (small-signal equivalent circuit for one-half of base region in an unsymmetrical junction diode at high injection levels)

From (49), (50), and (51)

$$R_3 = \frac{kT}{e I_{dc}} \frac{1 + \frac{H_c}{4 H_p} \left(1 + \frac{M_p}{M_n} \right)}{2 + \frac{H_c}{4 H_p} \left(1 + \frac{M_p}{M_n} \right)} \quad (52)$$

$$L = \frac{kT}{e I_{dc}} \frac{\frac{S}{4 H_p} \left(1 + \frac{M_p}{M_n} \right)}{2 + \frac{H_c}{4 H_p} \left(1 + \frac{M_p}{M_n} \right)} \quad (53)$$

The impedance of the bulk region $d/2 \leq x \leq d$ can be found from

$$\bar{Z}_{2,3} = \frac{\bar{V}_2 - \bar{V}_3}{\bar{I}} \quad (54)$$

The determination of $\bar{V}_2 - \bar{V}_3$ becomes cumbersome as a result of the high injection behavior near $x = d/2$ and the low injection behavior at $x = d$. Dill (1961) indicates that if the bulk region length is longer than the diffusion length for holes, the additional length is an unmodulated region that adds a non-inductive resistance to the diode. The diffusion length of holes is close to $d/2$ for the experimental diodes used in this thesis*, therefore, the remainder of the bulk region will be neglected.

If the equivalent circuits of the different parts (Figure 9 and Figure 10) are connected in series, the diode small signal equivalent circuit is obtained. This equivalent circuit shown in Figure 11 is valid for small signals applied to unsymmetrically doped junction diodes at high injection levels where the influence of the diffusion capacitance is dominated by the bulk inductance.

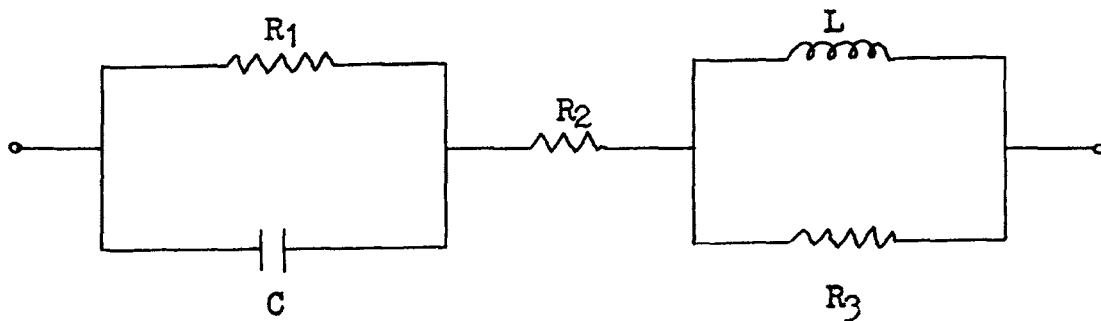


Figure 11. Small-signal equivalent circuit of an unsymmetrically doped junction diode at high injection densities.

* See Appendix for dimensions of experimental diodes.

CHAPTER VII

COMPARISON WITH EXPERIMENT

Figure 12 gives the results of impedance measurements taken to show the change over from capacitance dominated values at low injection levels to values dominated by the inductive effect at increasing injection current*. The change in θ from a negative to a positive angle is in agreement with the theory of inductance diodes as discussed in Chapter III. The decreasing value of $|Z|$

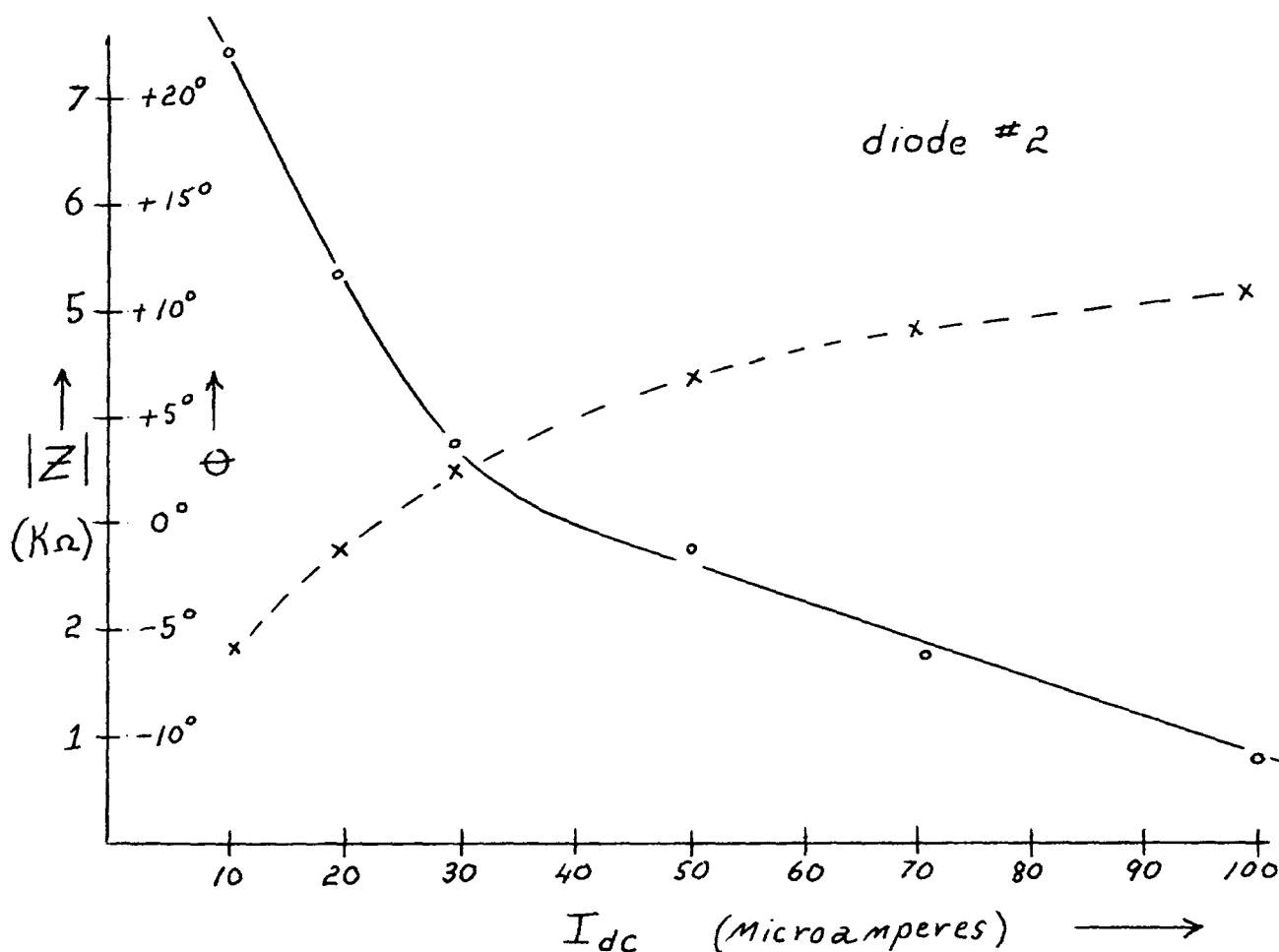


Figure 12. Impedance magnitude (solid line) and phase (dashed line) as a function of d-c current.

* See Appendix for tables of experimental and calculated data.

with increasing injection current is in agreement with equations (41) and (49) even though these equations were derived for high injection levels only.

Figure 13 compares the equivalent circuit performance to an experimental diode with base length approximately twice the diffusion length for holes. The displacement between calculated and experimental curves is most probably due to the neglecting of the unmodulated base region in Chapter VI. This nearly intrinsic bulk region adds resistance to the derived impedance expression. Figure 14 was obtained using a diode with base width approximately equal to $3 L_p$. Slightly more displacement between curves is observed thus substantiating the theory that the unmodulated base region should not have been neglected. The addition of more sections to the single-section lumped model would lead to better approximations.

No attempt is made to correlate the calculated and observed impedance phase angles as listed in Tables 2 through 5.

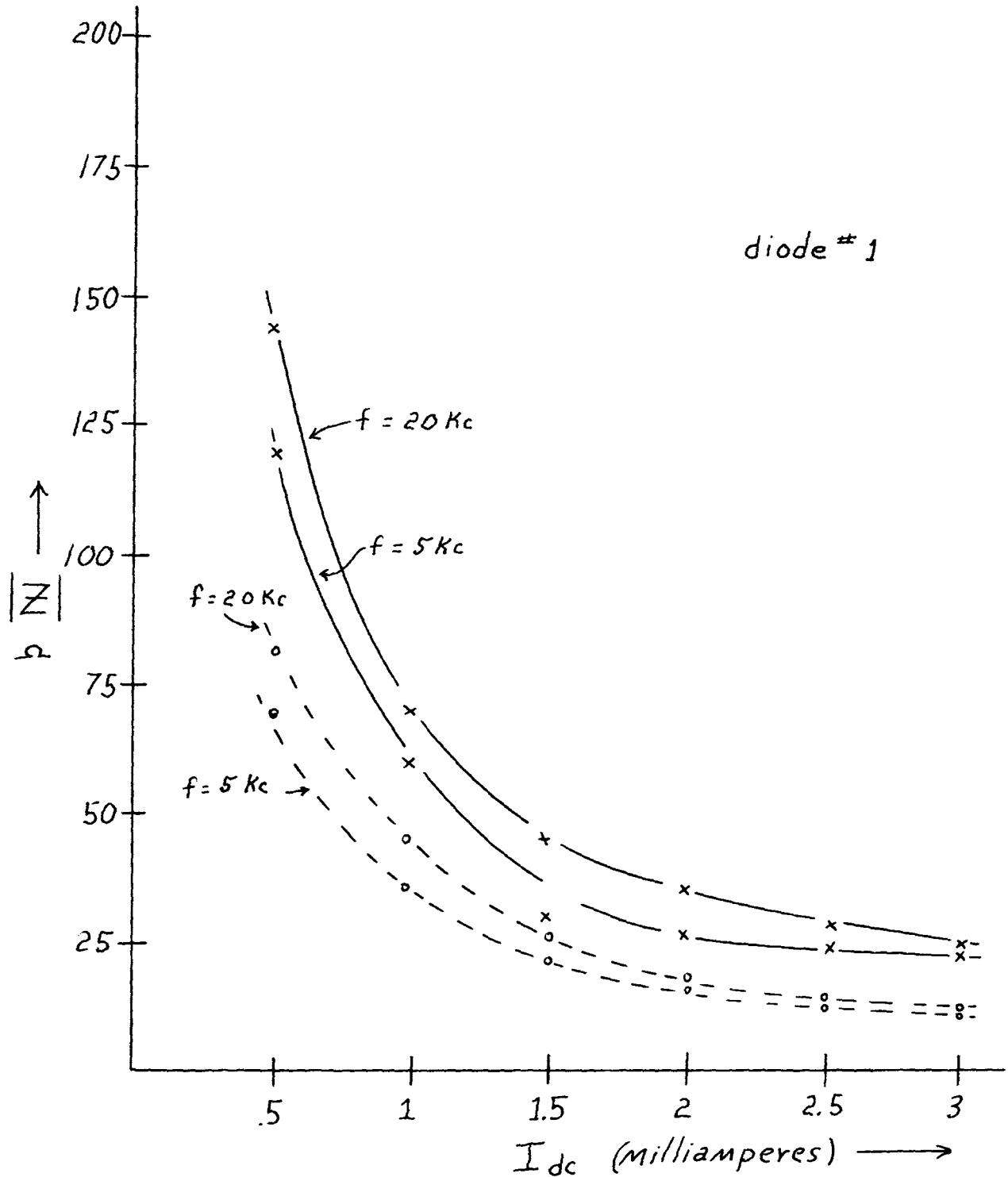


Figure 13. Small signal impedance magnitude of an unsymmetrically doped diode as a function of d-c current with frequency as a parameter. Full lines: measured impedance. Dashed lines: calculated impedance.

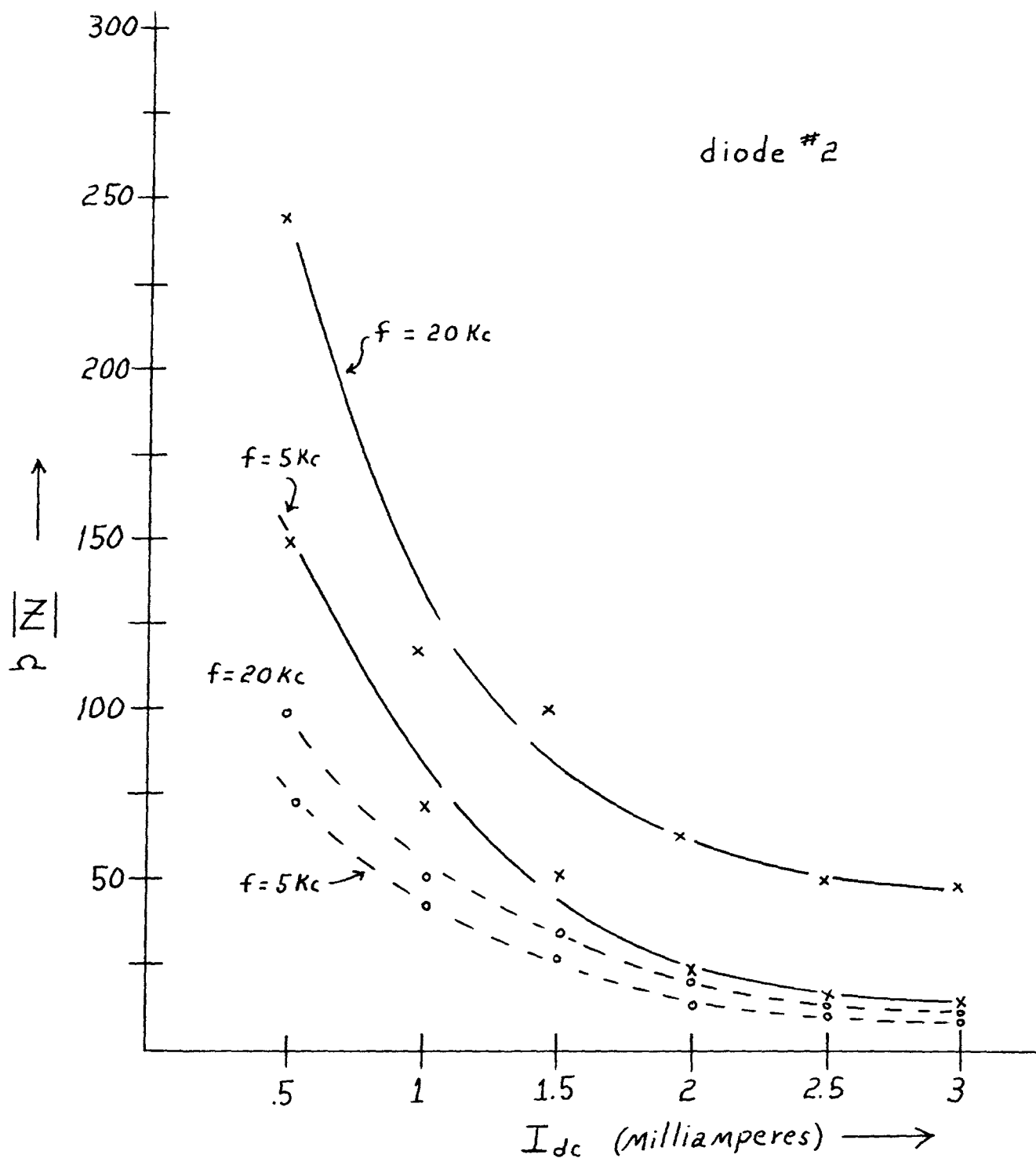


Figure 14. Small signal impedance magnitude of an unsymmetrically doped diode as a function of d-c current with frequency as a parameter. Full lines: measured impedance. Dashed lines: calculated impedance.

CHAPTER VIII

CONCLUSIONS AND RECOMMENDATIONS

It is concluded that the equivalent circuit of Figure 11 is valid for small-signals applied to unsymmetrically doped junction diodes at high injection levels where the influence of diffusion capacitance is dominated by the bulk inductance. The range of values of the capacitance and the parallel resistor R_1 is such that these terms could be neglected in many diodes of this type at high injection levels. For example, calculations using diode #1 resulted in capacitance values of .77 μf to 4.6 μf in parallel with .026 ohms to .0043 ohms respectively. It is also observed that even where unable to neglect these terms, the capacitance equation (46) can be reduced to

$$C = \frac{e I_{dc}}{k T} \frac{S}{4 H_p} \left(1 + \frac{M_p}{M_n} \right) \quad (55)$$

with very little error. Similarly equations (45) and (52) may be reduced to

$$R_2 = R_3 = \frac{k T}{e I_{dc}} \quad (56)$$

The calculations for an equivalent circuit of this type are tedious. It is recommended that any further work with the addition of more lumped models, be considered as a computer analysis. A suggestion for further work with this model is to investigate

the variation of inductive reactance with frequency. Ladany (1960) has predicted that the maximum inductive reactance occurs when the diffusion transit time equals the inverse of the radian frequency.

Another suggestion is the solution of equation (27) for the conditions of low and moderate as well as high current densities. This would lead to a more complete equivalent circuit of the inductance diode.

Questions were proposed in Chapter II as to what geometries and semiconductor properties could be optimized in order to enhance the inductance property. A large LC product will give a large ratio of inductive reactance to capacitive reactance. From equations (46) and (53)

$$LC = \left(\frac{S}{4 H_p} \right)^2 \frac{\left(1 + \frac{M_p}{M_n} \right)^2}{1 + \frac{H_c}{4 H_p} \left(1 + \frac{M_p}{M_n} \right)} \quad (57)$$

Replacing the Linvill parameters with their definitions, results in

$$LC = \frac{(\Delta x)^4}{16 D_p^2} \frac{\left(1 + \frac{\mu_p}{\mu_n} \right)^2}{1 + \frac{(\Delta x)^2}{4 \tau_p D_p} \left(1 + \frac{\mu_p}{\mu_n} \right)} \quad (58)$$

Since $(\mu_p/\mu_n) < \frac{1}{2}$

$$LC \approx \frac{(\Delta x)^4}{4 D_p [4 \tau_p D_p + (\Delta x)^2]} \quad (59)$$

This equation suggests that a material with a small diffusion constant and a long base width is desirable for inductance diodes. This is in agreement with equation (5) in the discussion of inductance diode theory.

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APPENDIX A

The "diodes" used for the experimental values were actually part of a 2N2160 unijunction transistor. Shown in Figure 15 is a sketch of the semiconductor regions as viewed through a metallurgical stage microscope. The germanium unijunction transistor was chosen because of the heavily doped p region and the long lightly doped n region. The emitter and base 1 were used as diode #1 and the emitter and base 2 as diode #2. Figure 16 is the circuit used to measure the impedance of the diodes.

The following physical constants for nearly intrinsic germanium are given by Linvill (1963) and were used in the calculations.

$$\begin{array}{ll}
 D_p = 49.3 \text{ cm}^2 \text{ sec}^{-1} & D_n = 101 \text{ cm}^2 \text{ sec}^{-1} \\
 \mu_p = 1,900 \text{ cm}^2 \text{ volt}^{-1} \text{ sec}^{-1} & \mu_n = 3,900 \text{ cm}^2 \text{ volt}^{-1} \text{ sec}^{-1} \\
 \tau_p = 20 \text{ u sec} & L_p = .3 \text{ mm}
 \end{array}$$

The Linvill parameters calculated from the measured dimensions and the above physical constants are:

<u>diode #1</u>	<u>diode #2</u>
$S = 1.5 \times 10^{-20} \text{ coulomb} \cdot \text{cm}^3$	$S = 2.5 \times 10^{-20} \text{ coulomb} \cdot \text{cm}^3$
$H_c = 7.5 \times 10^{-16} \text{ amp} \cdot \text{cm}^3$	$H_c = 12.5 \times 10^{-16} \text{ amp} \cdot \text{cm}^3$
$M_p = 5.3 \times 10^{-17} \text{ amp} \cdot \text{cm}^3/\text{volt}$	$M_p = 3.24 \times 10^{-17} \text{ amp} \cdot \text{cm}^3/\text{volt}$
$M_n = 11.1 \times 10^{-17} \text{ amp} \cdot \text{cm}^3/\text{volt}$	$M_n = 6.9 \times 10^{-17} \text{ amp} \cdot \text{cm}^3/\text{volt}$
$H_p = 1.4 \times 10^{-18} \text{ amp} \cdot \text{cm}^3$	$H_p = .86 \times 10^{-18} \text{ amp} \cdot \text{cm}^3$
$H_n = 2.86 \times 10^{-18} \text{ amp} \cdot \text{cm}^3$	$H_n = 1.75 \times 10^{-18} \text{ amp} \cdot \text{cm}^3$

The value of e/kT at room temperature is 38.5 volt^{-1} .

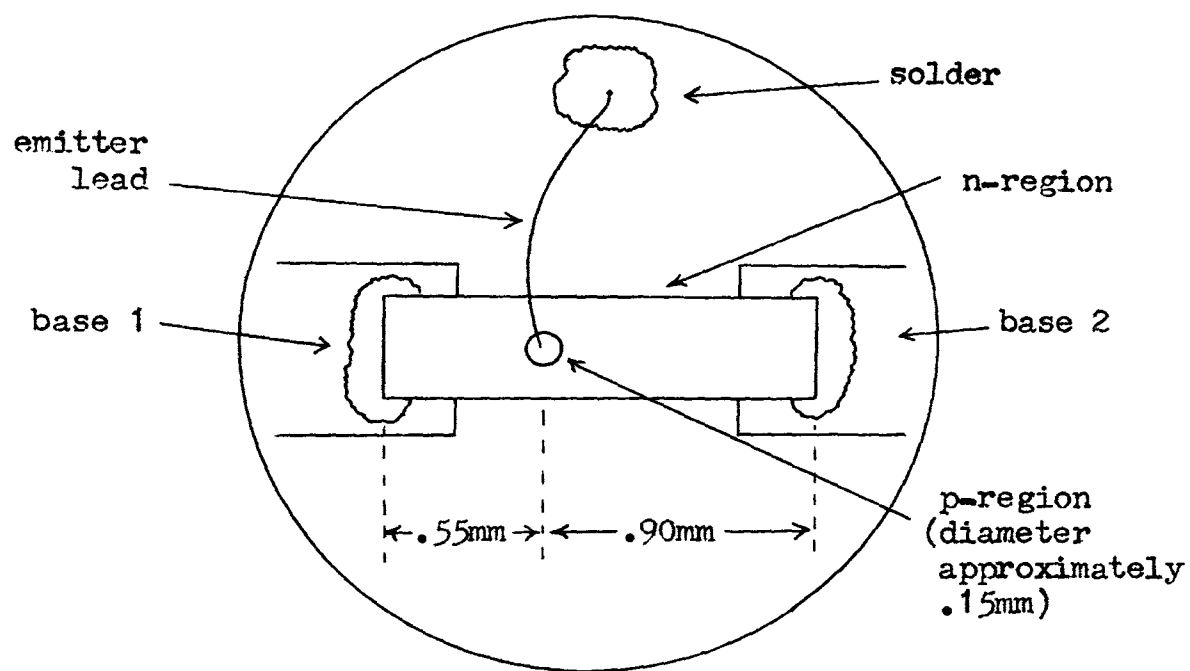


Figure 15. Semiconductor regions of a unijunction transistor as seen through a metallurgical stage microscope.

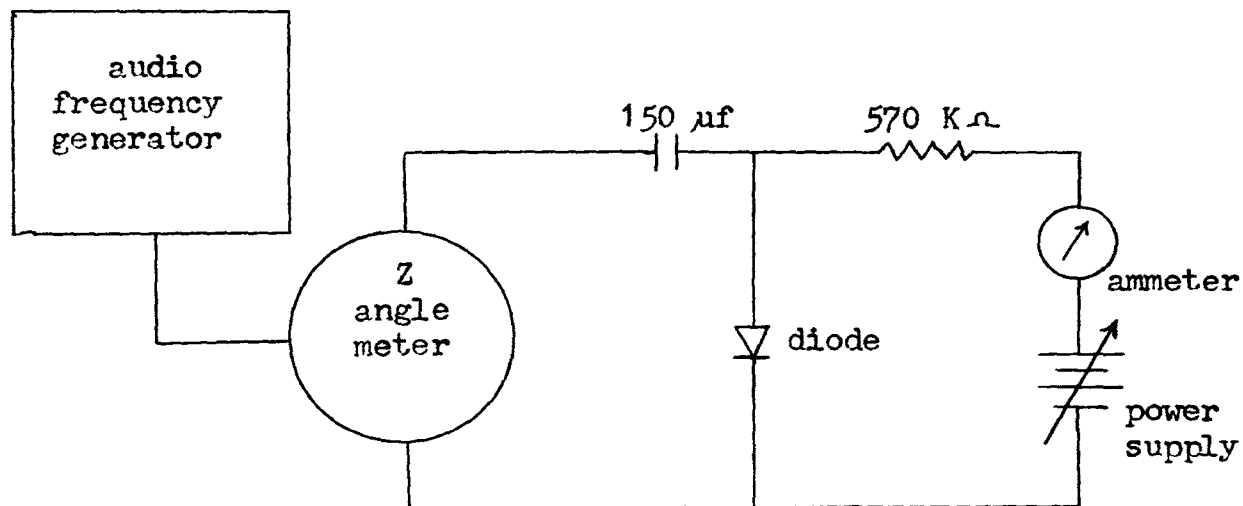


Figure 16. Circuit used to measure diode impedance

APPENDIX B

EXPERIMENTAL DATA

TABLE 1

Impedance magnitude and phase as a function of d-c current diode #2 frequency = 5 Kc						
I microamperes	10	20	30	50	70	100
$ Z $ kilohms	7.4	5.4	3.7	2.8	1.9	.875
θ degrees	-6°	-2°	+2°	+6°	+8°	+10°

TABLE 2

EXPERIMENTAL DATA

Impedance of diode #1 as a function of d-c current and frequency.			
I _{dc} (milliamperes)	Frequency (Kc)		
	5	10	20
.5	120 / <u>10°</u>	130 / <u>20°</u>	140 / <u>22°</u>
1	60 / <u>11°</u>	63 / <u>22°</u>	65 / <u>22°</u>
1.5	30 / <u>6°</u>	38 / <u>12°</u>	40 / <u>18°</u>
2	29 / <u>11°</u>	30 / <u>20°</u>	33 / <u>22°</u>
2.5	24 / <u>12°</u>	25 / <u>22°</u>	28 / <u>24°</u>
3	21 / <u>13°</u>	21 / <u>24°</u>	23 / <u>26°</u>

TABLE 3

EXPERIMENTAL DATA

Impedance of diode #2 as a function of d-c current and frequency			
I _{dc} (milliamperes)	Frequency (Kc)		
	5	10	20
.5	150 / <u>19°</u>	180 / <u>29°</u>	240 / <u>34°</u>
1	70 / <u>24°</u>	85 / <u>35°</u>	119 / <u>38°</u>
1.5	50 / <u>25°</u>	61 / <u>36°</u>	90 / <u>39°</u>
2	32 / <u>26°</u>	46 / <u>38°</u>	69 / <u>40°</u>
2.5	30 / <u>28°</u>	40 / <u>38°</u>	58 / <u>40°</u>
3	25 / <u>30°</u>	32 / <u>38°</u>	45 / <u>40°</u>

TABLE 4

CALCULATED DATA

Impedance of diode #1 as a function of d-c current and frequency		
I _{dc} (milliamperes)	Frequency (Kc)	
	5	20
.5	70.1 / <u>19.3°</u>	82.3 / <u>32.2°</u>
1	35 / <u>19.5°</u>	41.2 / <u>32.8°</u>
1.5	23.3 / <u>19.4°</u>	27.4 / <u>32.6°</u>
2	17.5 / <u>19.5°</u>	20.6 / <u>32.5°</u>
2.5	14 / <u>19.5°</u>	16.5 / <u>32.5°</u>
3	11.7 / <u>19.5°</u>	13.7 / <u>32.6°</u>

TABLE 5

CALCULATED DATA

Impedance of diode #2 as a function of d-c current and frequency.

I _{dc} (milliamperes)	Frequency (Kc)	
	5	20
.5	70 $\angle 19^\circ$	99 $\angle 10.5^\circ$
1	35 $\angle 19^\circ$	49.5 $\angle 10.6^\circ$
1.5	28.8 $\angle 19.2^\circ$	33 $\angle 10.6^\circ$
2	17.5 $\angle 19.4^\circ$	24.5 $\angle 10.6^\circ$
2.5	14 $\angle 19^\circ$	19.8 $\angle 10.6^\circ$
3	11.7 $\angle 19^\circ$	16.5 $\angle 10.6^\circ$

VITA

Donald Lawrence Willyard was born on September 21, 1935, near Viola, Missouri. He received his primary and secondary education in Blue Eye, Missouri.

The author served in the United States Marine Corps from 1954 to 1957. His Marine Corps duty included Naval Aviation Electronics School at Memphis, Tennessee and duty as a Radio/Radar Technician with the Marine Corps Airwing at El Toro, California. Upon release from active duty, he accepted employment as an Electronics Technician with the Boeing Airplane Company, Wichita, Kansas.

In February, 1960, the author entered the University of Missouri School of Mines and Metallurgy (now the University of Missouri at Rolla) from which he received the degree of Bachelor of Science in Electrical Engineering in July, 1962. In September, 1962, he accepted a faculty appointment as Instructor of Electrical Engineering and simultaneously began graduate study. In June, 1965, the author resigned from the teaching position to accept employment in the Semiconductor-Integrated Circuits Division of Texas Instruments Incorporated, Dallas, Texas.

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